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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
CHEN, JACK S J	

ART UNIT	PAPER NUMBER
2813	

DATE MAILED: 05/17/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

DETAILED ACTION

In response to the communication filed on November 21, 2003 through February 24, 2004, claims 9-15 are active in this application.

1. The reply filed on November 21, 2003 through February 24, 2004 is not fully responsive to the prior Office Action because of the following omission(s) or matter(s): Applicant states that applicants fully responded to the examiner's objection to the drawing on page 2-3 of applicant's November 21, 2003 reply, under the heading "objection to the Drawings," present applicants' position that the drawing (i.e., applicants' figure 1) sufficiently illustrates the claimed invention, and thus does not require the modification that the examiner requested. The Examiner disagrees because applicants have NOT complied with 37 C.F.R. § 1.83 (a); MPEP states "§ 1.83 Content of drawing. (a) The drawing in a nonprovisional application must show every feature of the invention specified in the claims. However, conventional features disclosed in the description and claims, where their detailed illustration is not essential for a proper understanding of the invention, should be illustrated in the drawing in the form of a graphical drawing symbol or a labeled representation (e.g., a labeled rectangular box)." In this case, the passivation layer covering the flash memory cell/floating gate is essential for a proper understanding of the invention. Further in this regard, it is noted that neither the applicants' specification nor the drawings requires the conductive layer 102 cover the flash memory cell having the floating gate and the passivation layer 103 covers the flash memory cell/floating gate. On the other hand, Applicants' disclosure merely shows forming the conductive layer on the substrate and forming the passivation layer on the conductive layer. Furthermore, according to fig. 1, only portions of the passivation layer cover the conductive layer or the substrate, and the position of the flash

memory cell having the floating gate is unclear (i.e., is the flash memory cell having the floating gate located under or above the opening/patterning portion of the passivation layer 103 or located on a different portion of the substrate? Is the metal layer 102 covering the flash memory cell having the floating gate? Is the flash memory cell having the floating gate formed on the conductive layer? And what's the location of the flash memory cell that was covering by the passivation layer according to applicants' claimed). Since the exact location of the flash memory cell having the floating gate is unknown; therefore, it is essential for a proper understanding of the instant claimed invention to show the claimed feature(s) and these conventional features should be illustrated in the drawing in the form of a graphical drawing symbol or a labeled representation (e.g., a labeled rectangular box), etc. See 37 CFR 1.111. Since the above-mentioned reply appears to be *bona fide*, applicant is given **ONE (1) MONTH or THIRTY (30) DAYS** from the mailing date of this notice, whichever is longer, within which to supply the omission or correction in order to avoid abandonment. EXTENSIONS OF THIS TIME PERIOD MAY BE GRANTED UNDER 37 CFR 1.136(a).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jack Chen whose telephone number is (571)272-1689. The examiner can normally be reached on Monday-Friday (9:00am-6:30pm) alternate Monday off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl W Whitehead can be reached on (571)272-1702. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jack Chen
Primary Examiner
Art Unit 2813